GAU- 2781
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. **RA001C9**)

In the Application of:

FARMWALD ET AL.

Serial No: 09/510,213

Filed: FEBRUARY 22, 2000

Title: METHOD OF OPERATING A MEMORY DEVICE HAVING A VARIABLE DATA INPUT LENGTH (AS AMENDED)

I hereby certify that this correspondence is being deposited with the United States Postal I Service as first class mail with sufficient postage in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on June 12, 2000
Michiko Sites
(Name of Person Mailing Correspondence)
Michiko Sites 6/12-2000
Signature Date

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, submitted herewith is a modified Form PTO-1449, including a copy of all of the documents listed therein.

Several of the documents listed in the PTO-1449 have been recently identified by a respondent in a pending ITC investigation, namely in re U.S. International Trade Commission Investigation No. 337-TA-431, Rambus Inc. vs Hitachi Ltd., et al., as prior art against the inventions claimed in U.S. Patent nos. 6,034,918 and 6,038,195, (hereinafter the '918 and '195 patents respectively). The '918 Patent, '195 Patent, and the instant application all relate back to the same Application -- App. Serial No. 07/510,898, filed April 18, 1990.

Kindly note, reference to the above-mentioned documents is made in paragraph 17 on page 28, as well as in Exhibit A, of the RESPONSE OF HITACHI LTD. TO THE COMPLAINT AND NOTICE OF INVESTIGATION (hereinafter the "RESPONSE"). A copy of the RESPONSE is submitted herewith.

It is respectfully requested that the Examiner make his consideration of these references formally of record with the next Office Action.

Respectfully submitted,

Date: June 9, 2000

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Atty. Docket No. RA001C9)

APPLICANT: **FARMWALD ET AL.** FILED: **February 22, 2000**
SERIAL NO.: **09/510,213**
TITLE: **METHOD OF OPERATING A MEMORY DEVICE HAVING A VARIABLE DATA INPUT LENGTH (AS AMENDED)**

RECEIPT OF THE FOLLOWING PAPERS IS ACKNOWLEDGED

1. Information Disclosure Statement (4 pages) + REFERENCES

DATE: **JUNE 12, 2000** ATTY: **NAS**

Invalidating Prior Art to the '195 and '918 Patents

This appendix is based upon Hitachi's current factual knowledge and understanding. Hitachi reserves the right to rely on and present additional invalidating prior art as to the '195 and '918 patents discovered in the course of this investigation.

1. Kawamasa, K.; "Memory Control Method"; Japanese Patent Application Kokai Publication No. S56-82961 (July 7, 1981).*

2. Taguri, J.; "Memory Storage Device"; Japanese Patent Application Kokai Publication No S57-14922 (January 26, 1982).*

3. Redwine et al.; "Semiconductor Read/Write Memory Array Having Serial Access"; United States Patent No. 4,330,852 (May 18, 1982).

4. Hasegawa, J.; "Memory System"; Japanese Laid Open Patent Application No. Sho 60-80193 (May 8, 1983).*

5. Miyazaki, Y.; "Block Transfer and Storage Control Method"; Japanese Laid-open Patent Application Sho 60-55459 (March 30, 1985).*

6. Hashimoto, S.; "Data Transfer Control System"; Japanese Patent Application Kokai Publication No. S61-72350 (April 14, 1986).*

7. Fischer, M.; "Fair Arbitration Technique for a Split Transaction Bus in a Multiprocessor Computer System"; United States Patent No. 4,785,394 (November 15, 1988).

8. Wantanabe, T.; "Session XIX: High Density SRAMs"; IEEE International Solid State Circuits Conference pp. 266-267 (1987).

9. James, D.; "Method and Apparatus for Performing Variable Length Data Read Transactions"; United States Patent No. 4,703,418 (October 27, 1987).

10. Taguchi, Y.; "Memory Device"; Japanese Patent Application Kokai Publication No. S63-142445 (June 14, 1988).*

11. Taguri, J.; "Memory Storage Device"; Japanese Patent Application Kokoku Publication No. B63-46864 (September 19, 1988).*

12. Horiguchi et al., "Semiconductor memory having error correcting means", United States Patent No. 4,726,021 (February 16,1988).

13. Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. Tech J., 24, 4, pp.293-300 (Dec. 1988).

14. Fast Packet Bus for Microprocessor Systems with Caches, IBM Technical Disclosure Bulletin, pp. 279-282 (January 1989).

15. Kumagai, T.; "Storage System"; Japanese Patent Application Kokai Publication No. S64-29951 (January 31, 1989).*

16. Gustavson, D.; "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb. 27-Mar. 3, 1989).

17. James, D.; "Scalable I/O Architecture for Buses"; IEEE, pp. 539-544 (April 1989).

18. Kimoto et al., "Micro-computer Capable of Accessing Internal Memory at a Desired Variable Access Time"; U.S. Patent No. 4,870,562 (September 26, 1989).

19. JEDEC SDRAM standards.

* Translation Included